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Embedded Systems – Lab 2: Interrupts and Timers

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PROJECT BASED LEARNING

Lab Structure

Topic of today's lab:

- Learn how interrupts and timers work in an MCU.

Agenda:

- 16:15 – 16:45 Introduction
- 16:45 – 18:00 Working on LAB tasks

Available Assistants: Filippo, Gabriel, Richard

Goal of this lab

- Configuration of **hardware interrupts**
- Interrupt vs. Polling
- Learn how to **debug** program running on a microprocessor
- Configuration of **hardware timers**
- Implementation of **pulse-width modulation (PWM)**

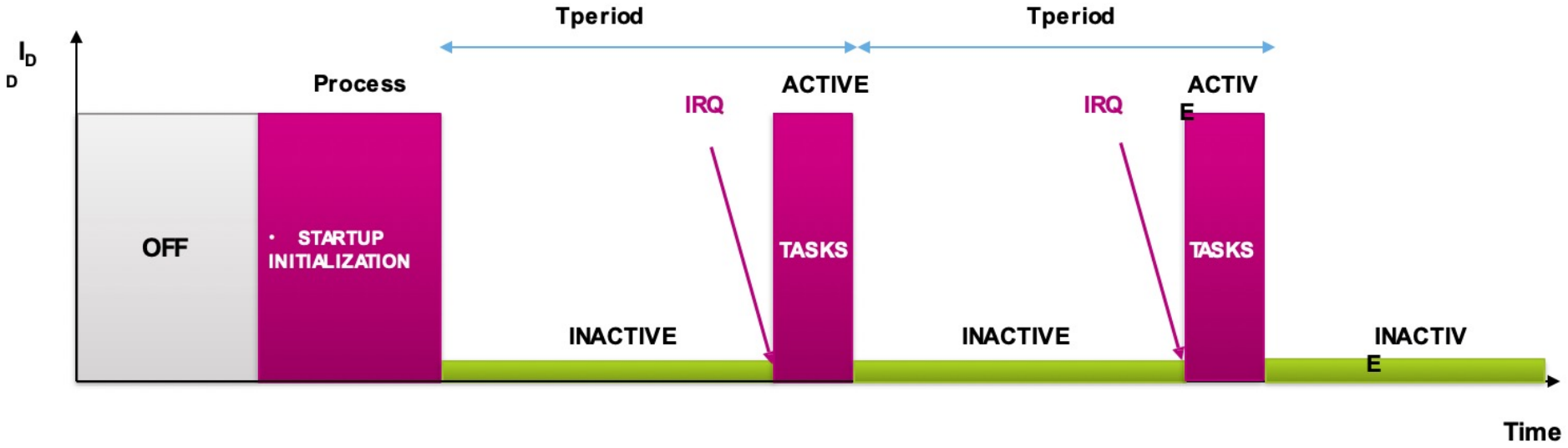
Interrupts

Polling

Are we there yet?
Are we there yet?
Are we there yet?
Are we the
Are we the
Are we the

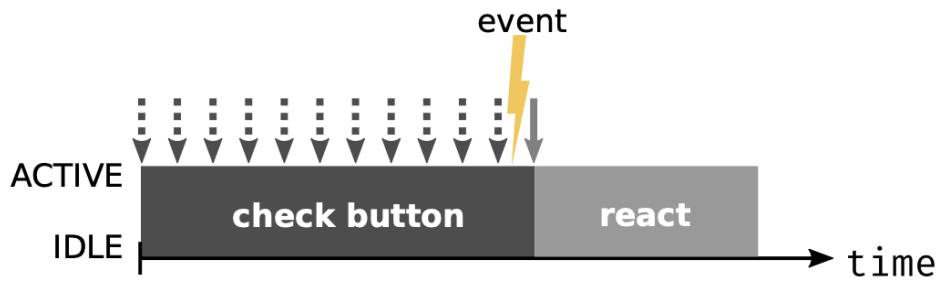
Interrupts

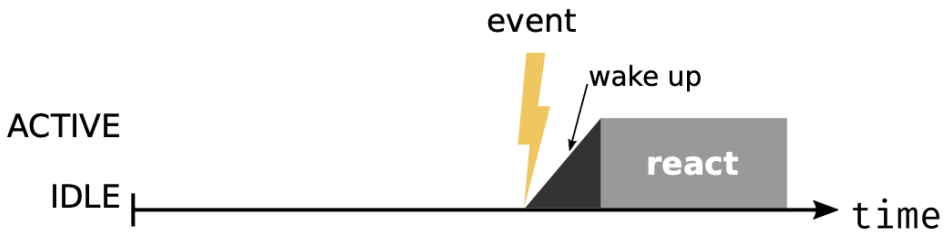
Wake me up when we get there...

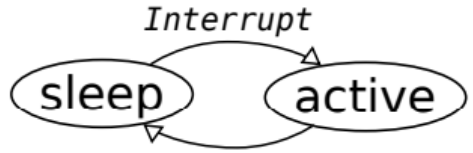


Interrupts

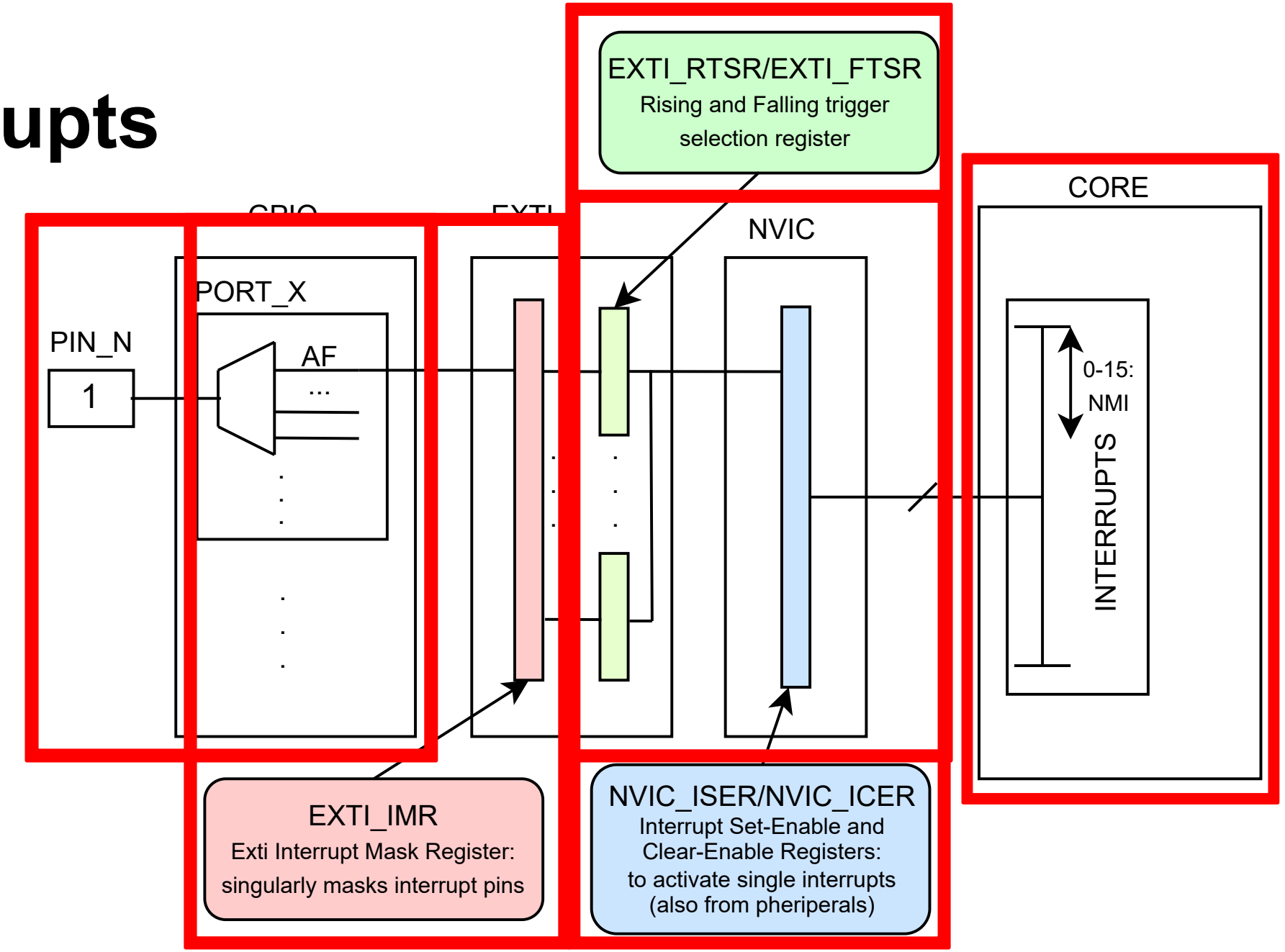
Definition: an hardware interrupt is an electronic signal that alerts the microprocessor of an event. An interrupt can be triggered by either an internal peripheral (e.g. timer) or an external device (e.g. button)







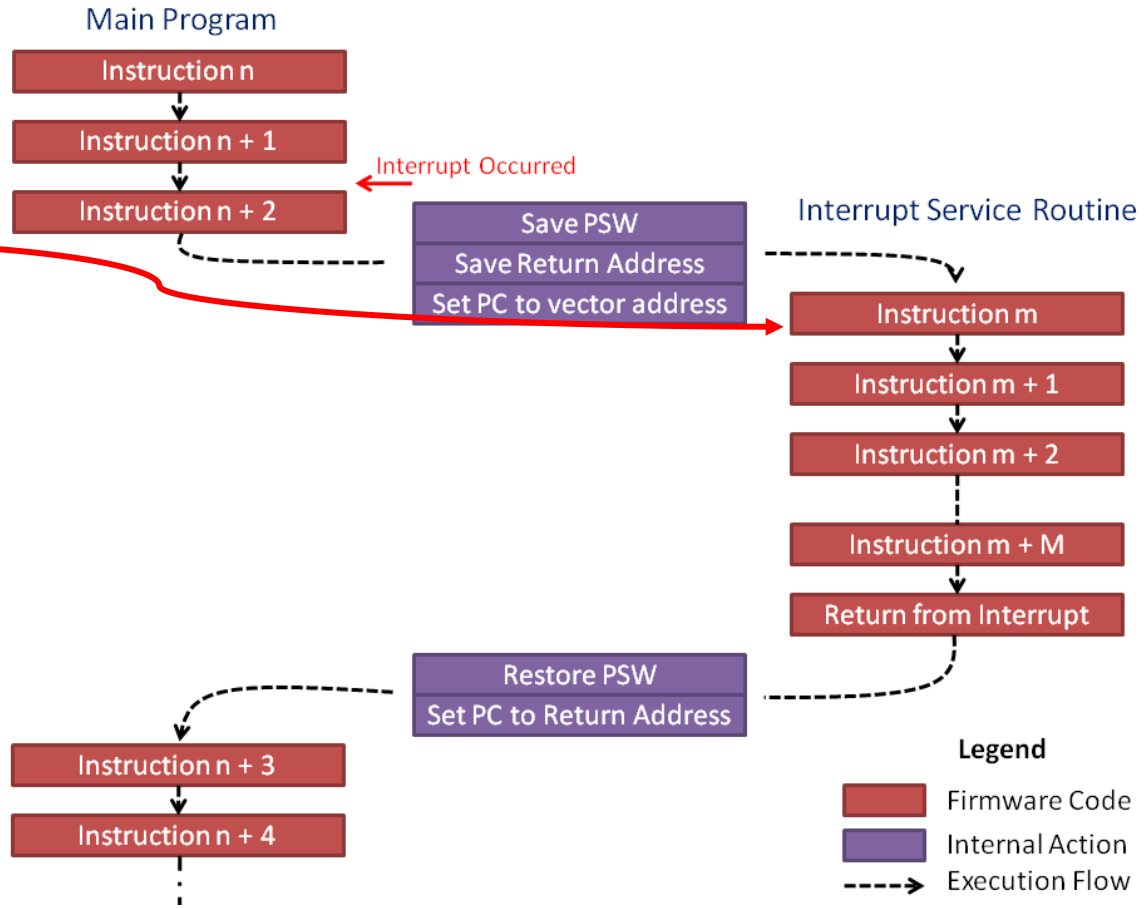
Interrupts


EXTI_RTSR/EXTI_FTSR
Rising and Falling trigger
selection register
CORE
NVIC
PORT_X
PIN_N
1
AF
...
0-15:
NMI
INTERRUPTS
EXTI_IMR
Exti Interrupt Mask Register:
singularly masks interrupt pins
NVIC_ISER/NVIC_ICER
Interrupt Set-Enable and
Clear-Enable Registers:
to activate single interrupts
(also from pheriperals)

Interrupts

Table 153. STM32U575/585 vector table

Position	Priority	Type of priority	Acronym	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	-4	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non maskable interrupt. The RCC clock security system (CSS) is linked to the NMI vector.	0x0000 0008
-	-3 or -1	Fixed	Secure HardFault	Secure hard fault	0x0000 000C
-	-1	Fixed	Non-secure HardFault	Non-secure hard fault. All classes of fault	0x0000 000C
-	0	Settable	MemManage	Memory management	0x0000 0010
-	1	Settable	BusFault	Pre-fetch fault, memory access fault	0x0000 0014
-	2	Settable	UsageFault	Undefined instruction or illegal state	0x0000 0018
-	3	Settable	SecureFault	Secure fault	0x0000 001C
-	-	-	-	Reserved	0x0000 0020 - 0x0000 0028
-	4	-	SVC	System service call via SWI instruction	0x0000 002C
-	5	-	Debug Monitor	Debug monitor	0x0000 0030
-	-	-	-	Reserved	0x0000 0034
-	6	Settable	PendSV	Pendable request for system service	0x0000 0038
-	7	Settable	SysTick	System tick timer	0x0000 003C



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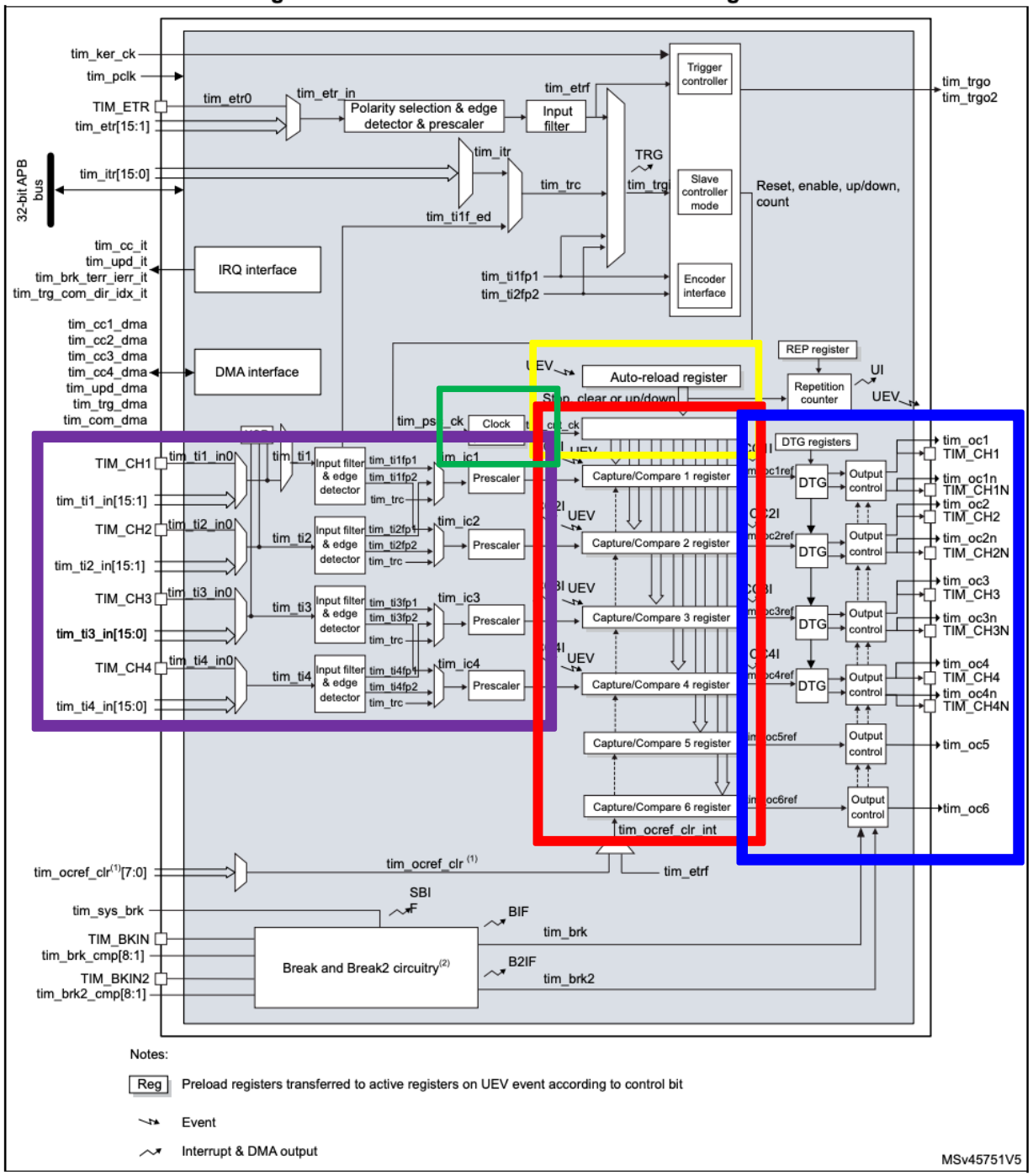
Timers

Figure 374. Advanced-control timer block diagram



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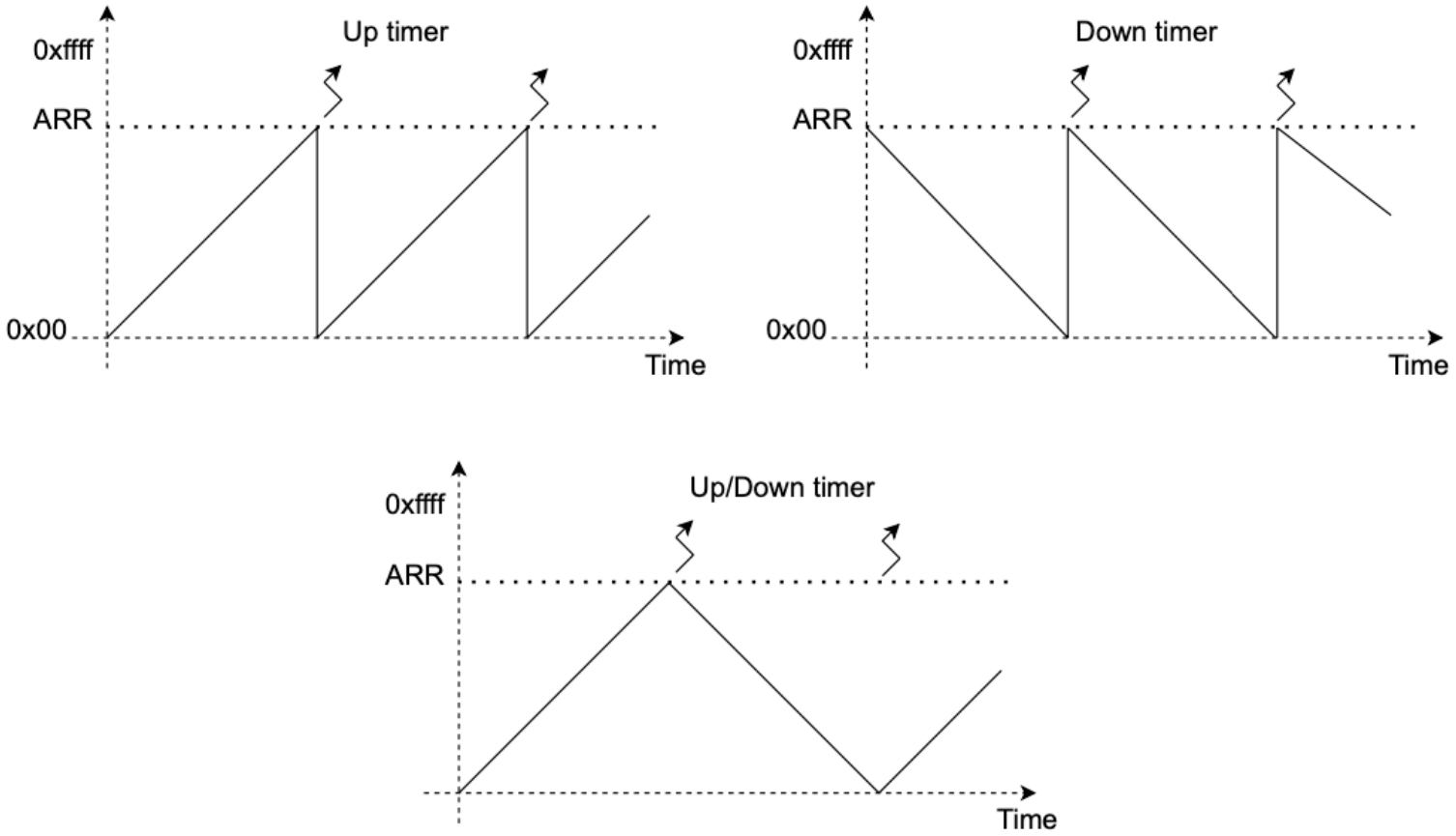
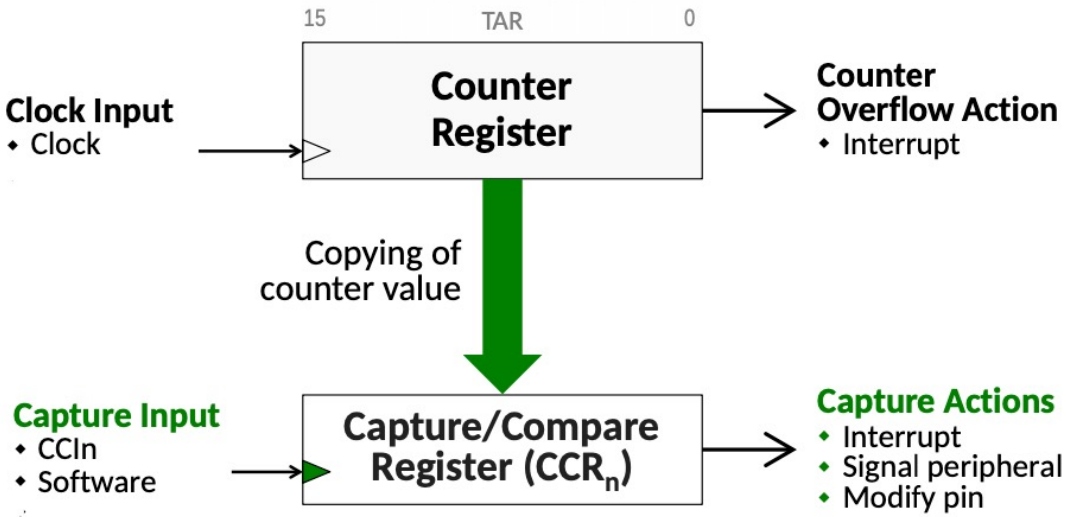
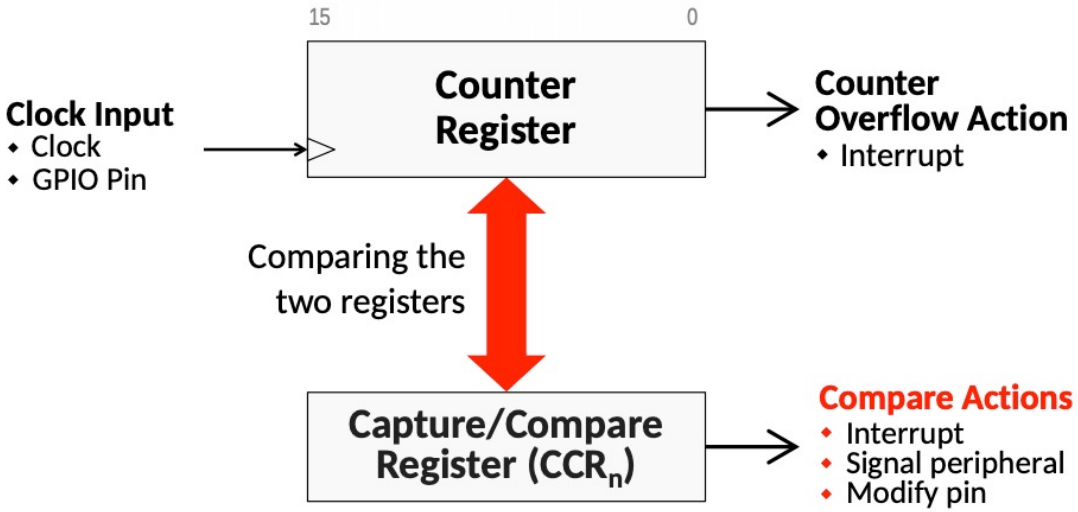
Timers – Up, Down and Up/Down

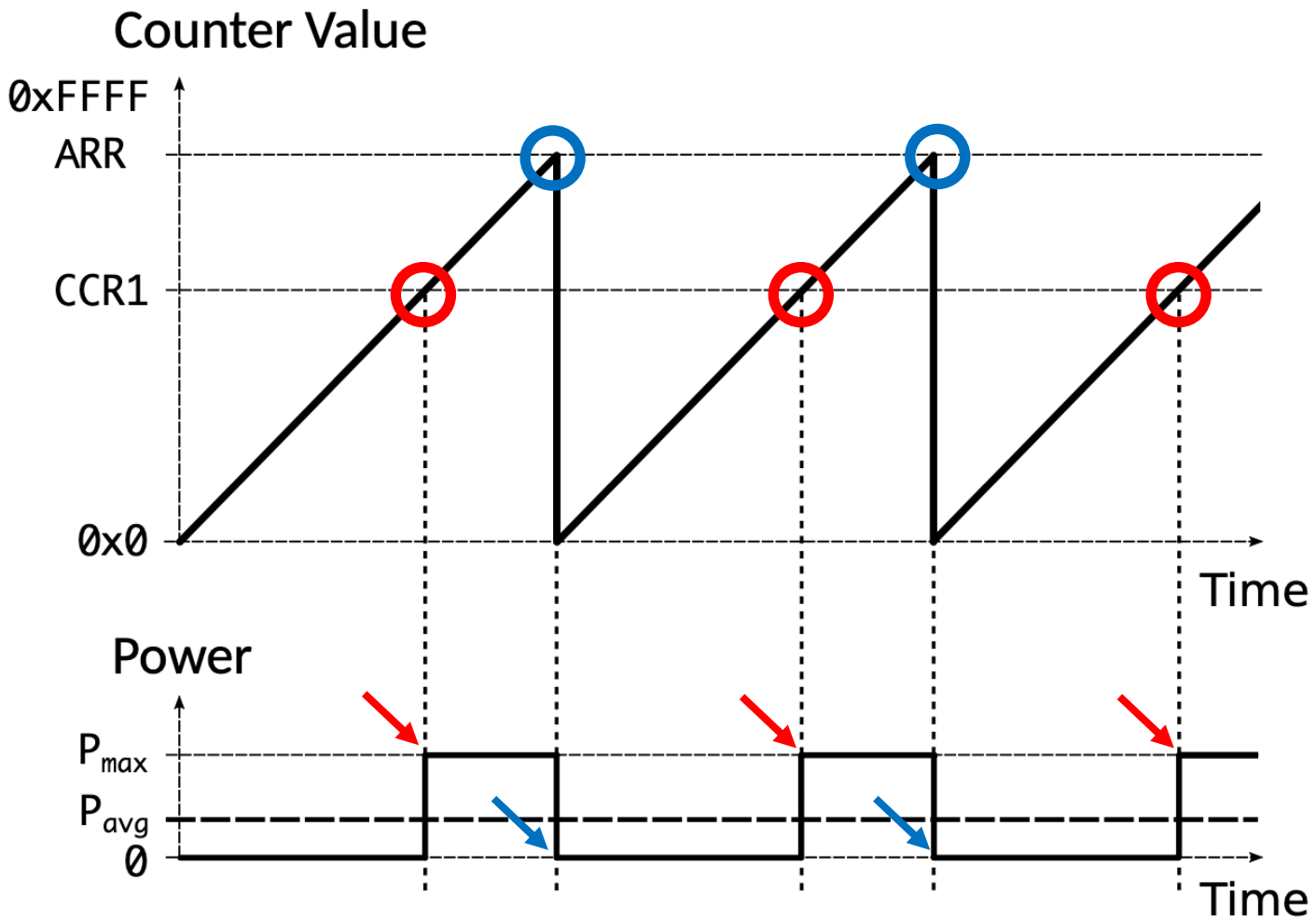


Timers – Input Capture and Output Compare





Timers - PWM


Counter Value
0xFFFF
ARR
CCR1
0x0
Time
Power
P_{max}
P_{avg}
0
Time

Tasks of Lab 2

- Task 1:
  - Interrupts
  - Debugging
- Task 2:
  - Timers
  - PWM

Tasks of Lab 2

- Introduction is over. Feel free to ask questions!
- The assistants are now available until 18:00 to answer questions.
- Email: For individual questions, you can also reach me under mgiordano@ethz.ch.
- On Friday from 16:15 - 18:00, we will repeat the session.

Happy coding!